Amendments to the Specification:

On page 9 of the application, please replace the full paragraph (line 20-21) with the following paragraph:

--~~Fig. 4 is a cross sectional view~~ Figs. 4(a) and 4(b) are cross sectional views of the plasma processing device of Embodiment 1 of the present invention.--

On page 10 of the application, please replace the full paragraph (lines 1-3) with the following paragraph:

--~~Fig. 6 is a schematic illustration~~ Figs. 6(a)-6(e) are schematic illustrations for explaining a process of method of manufacturing a semiconductor device of Embodiment 1 of the present invention.--

On page 10 of the application, please replace the paragraphs (lines 6-23) with the following paragraph:

--~~Fig. 8 is a schematic illustration~~ Figs. 8(a)-8(d) are schematic illustrations for explaining a step of plasma dicing in the method of manufacturing the semiconductor device of Embodiment 1 of the present invention.

~~Fig. 9 is a perspective view~~ Figs. 9(a)-9(c) are perspective views of a semiconductor wafer of Embodiment 2 of the present invention.

~~Fig. 10 is a schematic illustration~~ Figs. 10(a)-10(d) are schematic illustrations for explaining a step of plasma dicing

in the method of manufacturing the semiconductor device of Embodiment 2 of the present invention.

~~Fig. 11 is a schematic illustration~~ Figs. 11(a)-11(d) are schematic illustrations for explaining a step of plasma dicing in the method of manufacturing the semiconductor device of Embodiment 2 of the present invention.

~~Fig. 12 is a schematic illustration~~ Figs. 12(a)-12(d) are schematic illustrations for explaining a step of plasma dicing in the method of manufacturing the semiconductor device of Embodiment 2 of the present invention.--

On page 11 of the application, please replace the full paragraph (lines 3-21) with the following paragraph:

--Fig. 1 is a cross sectional side view of a plasma processing device of Embodiment 1 of the present invention, Fig. 2 is a partially cross sectional view of a lower electrode of the plasma processing device of Embodiment 1 of the present invention, Fig. 3 is a perspective view of a semiconductor wafer of Embodiment 1 of the present invention, ~~Fig. 4 is a cross sectional view~~ Figs. 4(a) and 4(b) are cross sectional views of the plasma processing device of Embodiment 1 of the present invention, Fig. 5 is a block diagram showing a constitution of a control system of the plasma processing device of Embodiment 1 of the present invention, ~~Fig. 6 is a schematic illustration~~

Figs. 6(a)-6(e) are schematic illustrations for explaining a process of method of manufacturing a semiconductor device of Embodiment 1 of the present invention, Fig. 7 is a flow chart of the plasma processing method of Embodiment 1 of the present invention, and ~~Fig. 8 is a schematic illustration~~ Figs. 8(a)-8(d) are schematic illustrations for explaining a step of plasma dicing in the method of manufacturing the semiconductor device of Embodiment 1 of the present invention.--

On pages 33-34 of the application, please replace the full paragraph (page 33, lines 18-page 34 line 11) with the following paragraph:

--The plasma processing device is composed as described above. Referring to ~~Fig. 6~~ Figs. 6(a)-6(e) and the other drawings, explanations will be made into the method of manufacturing the semiconductor device, in which the above plasma processing device is used, and the plasma processing method carried out in the process of the method of manufacturing this semiconductor device.--

On page 46 of the application, please replace the full paragraph (lines 1-10) with the following paragraph:

--~~Fig. 9 is a perspective view~~ Figs. 9(a)-9(c) are perspective views showing a semiconductor wafer of Embodiment 2 of the present invention. In Embodiment 1, two layers of SiO_2

layer 42 and the protective layer 43 are used as an etching stop layer. However, in this Embodiment 2, SiO_2 layer 42 or the protective layer 43 is singly used as an etching stop layer. Further, in this Embodiment 2, an electric conductive body used in the step of forming an active layer of the semiconductor element is used as an etching stop layer.--

On page 47 of the application, please replace the full paragraph (lines 12-22) with the following paragraph:

--Referring to ~~Fig. 10~~ Figs. 10(a)-10(d), the proceeding process of plasma dicing conducted on this semiconductor wafer 61 will be explained as follows. Fig. 10(a) is a view showing the semiconductor wafer 6 in the state before starting plasma dicing. The protective layer 43 is recessed and enters the groove-shaped gap 42b corresponding to the position of the cutting line 31b of cutting the mask. This recessed portion is the linear recessed portion 43b. The protective sheet 30 is attached to a surface of the protective layer 43 on the circuit forming face 61a side of the semiconductor wafer 61.--

On page 50 of the application, please replace the full paragraph (lines 15-24) with the following paragraph:

--Referring to ~~Fig. 11~~ Figs. 11(a)-11(d), the proceeding process of plasma dicing conducted on this semiconductor wafer

62 will be explained below. Fig. 11(a) is a view showing the semiconductor wafer 62 in the state before starting plasma dicing. The groove portion 43c is provided between the individual protective layers 43a corresponding to the position of the cutting line 31b of cutting the mask. The protective sheet 30 is attached to a surface of the individual protective layer 43a on the circuit forming face 62a side of the semiconductor wafer 62.--

On pages 53-54 of the application, please replace the full paragraph (page 53 line 24-page 54 line 8) with the following paragraph:

--Referring to ~~Fig. 12~~ Figs. 12(a)-12(d), the process of the progress of plasma dicing conducted on this semiconductor wafer 63 will be explained below. Fig. 12(a) is a view showing the semiconductor wafer 63 before the start of plasma dicing. The conductive layer 41a and the groove portions 42c, 43c are provided at positioned corresponding to the positions of the mask cutting lines 31b. The protective sheet 30 is attached onto a surface of the individual protective layer 43a on the circuit forming face 63a side of the semiconductor wafer 63.--

Please replace the Abstract of the Disclosure with the following revised abstract:

--In the process of plasma dicing in which the semiconductor wafer 6 is divided into individual pieces by

plasma, SiO_2 layer 42 and the protective layer 43, which are formed covering the active layer 41, are utilized as an etching stop layer for absorbing fluctuation of the etching rate in the first plasma dicing step in which the wafer base layer 40 is etched and cut off. Next, the second plasma dicing step is conducted in which the etching stop layer exposed by the first plasma dicing step is cut off with plasma of the second plasma generating gas capable of etching at a high etching rate, and heat damage is prevented which is caused when the protective sheet 30 is exposed to plasma for a long period of time.

~~[Selected Drawing] Fig. 8~~--

Attachment: Replacement Sheet